All answers must demonstrate an understanding of the problem and solution. Please show your work if you would like to receive partial credit. Explanations that are incorrect will affect your grade even if correct explanations are also present.

Print Name: __________________________________________
Problem 1: Short Answer

____________________________  (30)

Problem 2: Verilog

____________________________  (10)

Problem 3: Caches and Virtual Memory

(a) __________________________  (5)
(b) __________________________  (5)
(c) __________________________  (5)
(d) __________________________  (5)

Problem 4: Scheduling and Prediction

(a) __________________________  (5)
(b) __________________________  (5)
(c) __________________________  (5)
(d) __________________________  (5)
(e) __________________________  (5)

Problem 5: ILP

(a) __________________________  (5)
(b) __________________________  (10)

Extra Credit

____________________________  (10)

Total: _________________________
1. Short Answer (30 points, 2 points each)

a). A machine with a lower CPI is always faster than a machine with a higher CPI.
   i) True
   ii) False

b). List two reasons why modern processors need virtual memory.

c). Will adding additional integer execution pipes guarantee higher performance in a superscalar processor? Explain in one sentence.

d). Name one advantage and one disadvantage of adding more stages to a microprocessor pipeline.

e). Does using predication eliminate the need for conditional branches? Why or why not?

f). Is it possible for an unrolled loop to run slower than the original loop? Why or why not?

g). What is the one major difference between Scoreboarding and Tomasulo's Algorithm?
1. Short Answer (cont’d)

h). What is the smallest positive number (> 0) you can represent in normalized form in IEEE floating point single-precision format? Show the number in scientific notation and also show clearly how the number is stored in each field of the single precision IEEE format.

i). How many bits per entry are necessary in a direct-mapped branch-target buffer with 2K entries assuming the machine has word-aligned instructions, a 40-bit PC, and a separate branch prediction mechanism?

j). State a difference between the IA-64 architecture and a VLIW machine.

k). Name two architectural structures that have to change in a traditional out-of-order processor to accommodate SMT.

l). What is the purpose of register renaming?

m). Is it better to halve the miss rate or the miss penalty of an L2 cache?
1. Short Answer (cont’d)

n). Why does the Alpha tournament branch predictor perform better than a gshare predictor?

o). Give 2 advantages and 2 disadvantages of large page sizes.